Report on VLSI Design Review II

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1 Completed Work

- **Function Verification:** In previous literature review, we collected existed typical priority encoder circuit designs. According to our research plan, function verification was implemented first to prove the validity of such circuits. Meanwhile, we could better understand the designs, and hopefully, get some inspiration to a new design with better performance. Through Cadence simulation, we verified the function of all those circuits and had a good understand of their design idea.
- **Measurement of Energy-Consumption and Delay:** In this project, circuit power consumption and delay are the major metrics we are concerned of. Through Cadence simulation, we are able to measure 5 typical priority encoders' power and delay performance using the same NCSU_Devices_FreePDK45 technology to provide fair comparison. Specifically, to measure the power consumption for each circuit, we average the power for all input combinations and for delay measurement, we analyze the circuits to obtain the inputs and outputs than lead to worst-case delay and then measure delays accordingly.
- **Comprehensive Literature Search on Priority Encoder Designs:** In previous review, we included 6 different priority encoder designs. Now, with the first reported priority encoder design included, we could have a complete comparison among all typical priority encoders in the past 16 years from 1998 to 2014.
- **Power and Delay Modeling:** Through Cadence simulation, we could measure power consumption and delay of existed circuits. Another approach to estimate these metrics is through formula derivation, which requires modeling of circuit power and delay. In recent work, we found certain relative papers in this area. Among them, paper [2] and [3] provided good approaches to model the delay and power consumption in VLSI, which could be implemented in our project. The summary of these two papers is included in the reference summary part attached with this design review.

2 Remaining Tasks

- **Performance Disparity Analysis:** Based on the measured delay and power consumption of existed priority encoders, try to identify reasons of their performance disparity.
- **8-Bit Priority Encoder Design:** Design a new priority encoder with better performance in terms of delay, power consumption or complexity.
- **Performance Estimation** Try to derive formulas to estimate delay and power performance and then find out their accuracy compared to simulation results.

3 Challenges and Questions

- **Cadence Simulation:** Due to the fact that a typical 8-bit priority encoder consists of about one hundred transistors, to simulate their performance using Cadence requires a fair amount of skills and focus.
- **New priority encoder design:** Since priority enders have been extensively studies since 1990s and there have been various designs aiming to improve delay, power or/and area performance, trying to design a new priority encoder with better performance is quite challenging.
- **Delay and Power Estimation by Formulation:** For a typical 8-bit priority encoder, there are usually near one hundred transistors involved, which makes the modeling of parasitics very complicated and the accuracy of mathematical estimation would be compromised.

We've accomplished around half of the tasks identified in our proposal. Since the time left to the final presentation is quite limited, we plan to devote more time to realized our goals on time.

Reference

[1] Jose G. Delgado-Frias and Jabulani Nyathi, "A VLSI high-performance encoder with priority look-ahead." Proceedings of the 8th Great Lakes Symposium on VLSI, 19-21 Feb 1998, pp. 59 - 64

[2] Ousterhout, John K. "Switch-level delay models for digital MOS VLSI." ACM Papers on Twenty-five years of electronic design automation, 1988.

[3] Liu, Dake, and Christer Svensson. "Power consumption estimation in CMOS VLSI chips." IEEE Journal of Solid-State Circuits, 29.6 1994, pp. 663-670.